Chapter XI
A 2.4-GHz Direct Conversion Transmitter for WiMAX and WiBro Applications

By Cecile Masse

As the 802.11 Wireless LAN market matures and with the adoption of the 802.16 WiMAX Standard, there has been a growing interest in technologies that allow delivery of higher data rates over large geographical areas. The IEEE 802.16 family of standards (802.16-2004 and 802.16e) are intended to provide high bandwidth wireless voice and data for residential and enterprise use. The modulation used to achieve these high data rates is OFDM (Orthogonal Frequency Division Multiplexing). WiMAX OFDM features a minimum of 256 sub-carriers up to 2048 sub-carriers, each modulated with either BPSK, QPSK, 16QAM or 64QAM modulation. Self interference is minimized by having these carriers orthogonal to each other. This standard also supports different signal bandwidths, from 1.25 MHz to 20 MHz to facilitate transmission over longer ranges and to accommodate different multipath environments. This represents a significant increase in systems profiles complexity as compared to the Wi-Fi 802.11 standard, mostly to guarantee a wider, more efficient, more robust network. More sub-carriers and variable length guard intervals contribute to this enhancement.

The composite signal envelope amplitude of the OFDM signal can exhibit significant peaks and valleys, so, theoretically, there is a possibility that the signals on each individual carrier reach their peaks at the same time, contributing to a peak-to-average ratio (PAR) of 10 * log(256) = 24 dB. In practice, WiMAX 256-OFDM exhibits a PAR of about 12 dB. Still, this imposes significant constraints on the transmitter's linearity, and requires large power back-off. On the other hand, the higher the transmitted signal data rate is, the higher the signal-to-noise ratio (SNR) requirement for the transmitter and receiver becomes. In 64QAM OFDM, the limited symbol decision area dictates an SNR of at least 30 dB. This SNR requirement can easily be translated into an EVM specification equivalent to the total amount of amplitude and phase distortion. For 64QAM, the equivalent EVM specification is –31.4dB or 2.7%. This challenging specification imposes very low phase noise for the LO, as well as tight I and Q matching before the up-conversion.

Many licensed or un-licensed RF bands, ranging from 0.7 GHz to 5.8 GHz, have been identified for WiMAX applications. But most of the initial designs are targeting frequency bands at 2.5 GHz and 3.5 GHz. WiBro is the Korean WiMAX mobile standard in the 2.3 GHz to 2.4 GHz band. This article proposes a direct-conversion transmit signal chain for this particular band of interest. Measurement results are also presented which demonstrate system level performance for WiMAX applications.

Architecture

To address the challenging requirements of the 802.16 standard, the transmit signal chain may be based on radio architectures like superheterodyne, IF sampling or zero-IF.

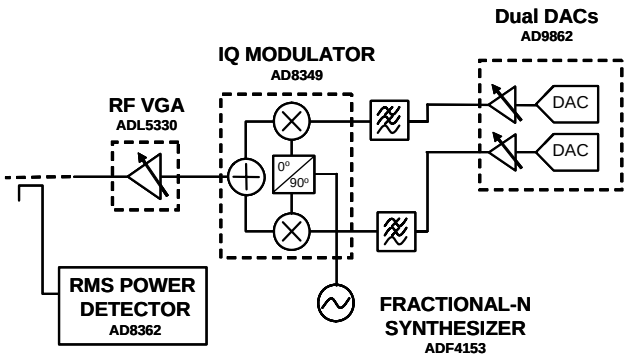

Fig 1. Architectural Block diagram

At 2.35 GHz, a direct up-conversion architecture is attractive for the following reasons: state of the art synthesizers and IQ modulators still perform well at this frequency, WiMAX OFDM has no active sub-carrier at the origin, direct up-conversion produces less mixing product spurs, it requires fewer filters which is important when dealing with wideband signals, and the lower number of parts helps minimize the current consumption. Finally, in multi-carrier modulation schemes like WiMAX OFDM, reducing the number of LO mixes is critical. The high number of sub-carriers within the OFDM signal actually makes this modulation quite sensitive to phase noise, as each of the N sub-carriers will be modulated by the phase noise of the LO.

Figure 1 shows a block diagram of the proposed TX signal chain architecture. The I and Q analog baseband signals are generated by a dual 14-bit DAC. The direct RF up-conversion is done using an IQ modulator. Low-pass filters are required at the DAC output to remove

the alias at the sampling frequency before the up-conversion.
The LO is generated by an external fractional-N synthesizer, which provides a continuous wave signal with minimal phase error. Finally, the composite RF output signal is amplified or attenuated through a variable gain amplifier (VGA) with a 50-dB of gain control range. An rms power detector ensures precise control of the output power.

Transmitter Implementation

BASEBAND SIGNAL GENERATION

The performance of the DAC is critical when dealing with the wideband OFDM signal. The signal-to-noise-ratio (SNR) and sampling rate define the spectral purity and signal quality of the modulated signal driving the IQ modulator.

The DAC resolution should provide sufficient dynamic range to meet the spectral mask at maximum output power and EVM at the lowest power levels. For instance, a SNR of 31.4 dB + margin is required for 64QAM ¾ OFDM, even at the minimum output power at the antenna. The target SNR for this design is 60 dB or better, and the chosen AD9862 14-bit DAC provides better than 70 dB SNR.

The maximum modulation bandwidth addressed in these WiMAX applications also dictates the appropriate sampling frequency. In this design, a 10 MHz complex OFDM signal requires a sampling frequency of at least 20 MHz. But all sampling images would be at N*20 MHz (N>0), which would fall in-band for an RF system with bandwidth higher than 20 MHz.

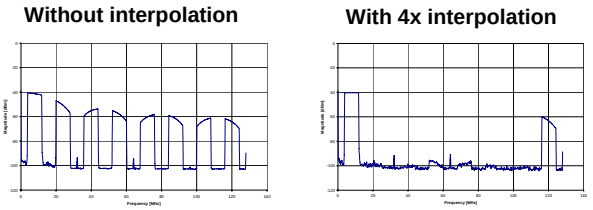

Figure 2. DAC Images with and without Interpolation

Choosing a DAC with an integrated interpolation filters helps relax the design of the off-chip reconstruction filter. For this architecture, while the TX digital data is updated at a rate of 20 MHz, the 4× interpolation filter effectively increases the overall sampling rate to 80 MHz. On the other hand, the relative level of the images at N*Fs also drops as a result of this increase in sampling rate. These amplitude levels are determined by the sin(x)/x roll-off from the sample-and-hold action of the DAC.

$$V_{out}(f) = V_{sampled}(f).\left(\frac{\sin(\pi fT)}{\pi fT}\right)$$

The off-chip anti-alias low-pass filter can then be designed with a relatively low order. Bessel filters are ideal for their flat in-band group delay, flat pass-band response, and limited in-band distortion. The order is chosen depending on the sampling frequency (Fs) and the required rejection at n*Fs.

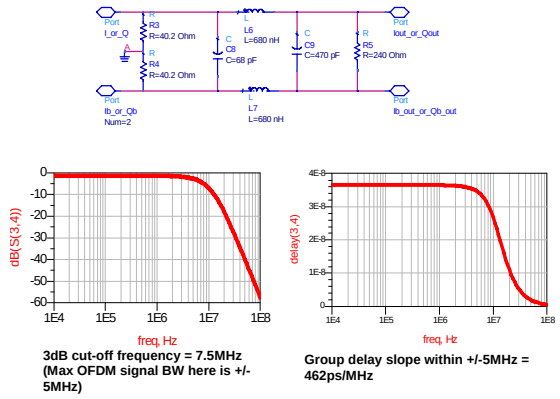

Figure 3. Baseband Bessel Low Pass Filter

At a sampling frequency of 80 MHz, the measured levels of the sampling images were
–33 dBc for the first image and –40 dBc for the second image. A third-order anti-alias low pass filter with a 3-dB cut-off frequency of 8 MHz provides 50 dB of rejection at 80 MHz, bringing the sampling images down to 80 dBc.

UPCONVERTER

The AD8349 is a fixed gain silicon, monolithic, RF quadrature modulator that is designed for use from 700 MHz to 2700 MHz. The differential or single-ended LO input signal is buffered, and then split into an in-phase (I) signal and a quadrature-phase (Q) signal using a polyphase phase splitter. These two LO signals are further buffered and then mixed with the corresponding I channel and Q channel baseband signals in two Gilbert cell mixers. The mixers' outputs are then summed together in the output amplifier. The output amplifier is designed to drive 50 Ω loads.The RF output can be switched on and off within 50 ns by applying a control pulse to the ENOP pin.

The AD8349 can be used as a direct-to-RF modulator in digital communication systems such as GSM, CDMA, and WCDMA base stations, and QPSK or QAM broadband wireless access transmitters. Its high dynamic range and high modulation accuracy also

make it a perfect IF modulator in local multipoint distribution systems (LMDS) using complex modulation formats.

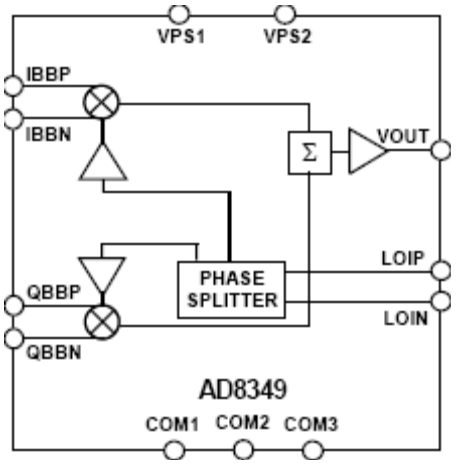

Figure 4. AD8349 700 MHz to 2700 MHz Quadrature Modulator

The Peak-to-Average Ratio of the 256-OFDM WiMAX modulation can reach 12 dB. For optimum spectrum quality out of the modulator, the appropriate peak voltage for the I and Q signals needs to be determined. The modulator used in this signal chain provides 0 dBm of rms output power for 1.2 Vpp of I and Q input drive level. Besides, the OP1dB of the modulator is 5 dBm. A 15 dB back-off provides optimum spectrum performance for the WiMAX OFDM signal, equivalent to an ac input level for the IQ modulator of about 750 mVpp differential.

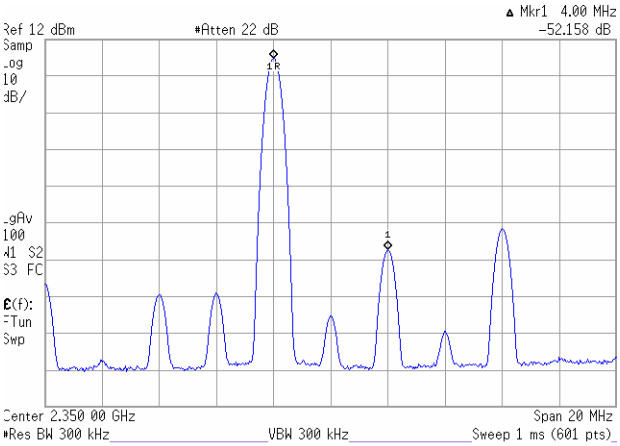

Figure 5. I/Q DC offset correction and sideband nulling.

With modulation schemes such as WiMAX OFDM, it is important to correct for the modulator mismatches that directly impact EVM performance. Amplitude and phase mismatches between I and Q signals, and an imprecise 90° LO phase shift within the IQ modulator, will result in an unwanted upper sideband image at LO+BB, when the wanted signal is at LO–BB. When the TX DACs are configured for complex outputs, good image rejection at the modulator output is critical because this spur falls inside the wanted channel. Phase mismatches cannot easily be compensated for, but amplitude matching can be achieved through independent gain correction at the DAC level. In this design, the DAC integrates a gain calibration function that allows the output current on either I or Q channels to be changed by up to 20 dB with a fine resolution of ±4%. A total image rejection of 50 dBc minimum is required to guarantee good EVM performance, and this gain correction circuit meets the requirement with margin.

LOCAL OSCILLATOR

Because the transmitter uses a zero-IF topology, the most appropriate synthesizer architecture for LO generation is a fractional-N PLL. Performance such as phase noise at 2.35 GHz, frequency resolution, and settling time drive the choice of the synthesizer architecture.

In the up-conversion, phase noise is superimposed on each of the N sub-carriers of the WiMAX OFDM signal when mixed to the local oscillator.

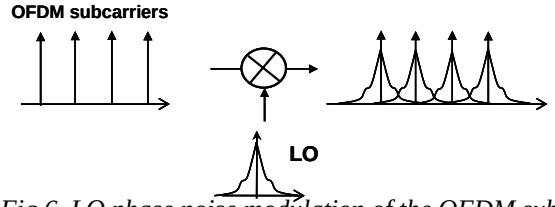

Fig 6. LO phase noise modulation of the OFDM sub-carriers

Compared to 802.11 Wi-Fi systems, the carrier spacing is also much narrower because of the higher number of sub-carriers within a given channel bandwidth. As an example, for a 20-MHz channel bandwidth, the carrier spacing in 802.11 is 385 kHz, compared to 78 kHz in 802.16d. Integrated phase error within the OFDM signal then becomes significantly higher, which directly contribute to the degradation of EVM. Although the OFDM symbol contains eight pilot tones that help a receiver track and remove most of the close-in phase noise generated by the LO, the standard still requires stringent EVM to be met at the antenna. For a 64QAM modulated OFDM, the EVM specification at the transmitter output is 2.7% rms. The PLL loop bandwidth and total integrated phase error are thus critical to the design of this PLL. A total phase error

lower than 1 degree rms has been used as a criteria for choosing and designing the LO synthesizer.

A fractional-N synthesizer inherently has very good phase noise compared to an integer-N architecture. Very high frequency resolution can be achieved while using a higher comparison frequency, therefore helping reduce the total phase noise. For a frequency resolution of 125 kHz, an output frequency of 2350.125 MHz could be synthesized with a 10 MHz reference frequency:

$$F_{out} = \left(N + \frac{K}{\frac{F_{PFD}}{F_{RES}}} \right) \times F_{PFD} = \left(235 + 1.\frac{125kHz}{10MHz} \right).10MHz = 2350.125MHz$$

The typical phase noise error for these fractional-N synthesizers can be less or equal to 0.5 degree rms, which is appropriate for this application.

The ADF4153 is a fractional-N frequency synthesizer that implements local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a Σ-Δ based fractional interpolator to allow programmable fractional-N division. The INT, FRAC, and MOD registers define an overall N divider (N = (INT + (FRAC/MOD))). In addition, the 4-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a voltage controlled oscillator (VCO).

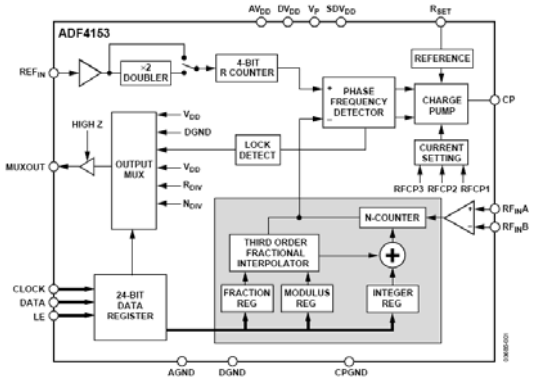

Figure 7. ADF4153 4 GHz Fractional-N Synthesizer.

A simple 3-wire interface controls all on-chip registers. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

In this particular system, the PLL has been designed with a closed loop bandwidth of about 20 kHz. For a 10-MHz WiMAX OFDM signal, the symbol duration is 25.6 µs, which corresponds to a sub-carrier spacing of 39 kHz. The PLL loop has deliberately been designed slower than the symbol duration so that most of its phase noise can be tracked and removed by the pilot tracking algorithm within the demodulator.

For non frequency-hopping TDD applications, PLL lock time is not that critical, as both transmitter and receiver operate at the same channel frequency. Therefore, designing a fast wideband PLL loop is not necessarily required. Figure 3 shows the simulated closed loop phase noise performance.

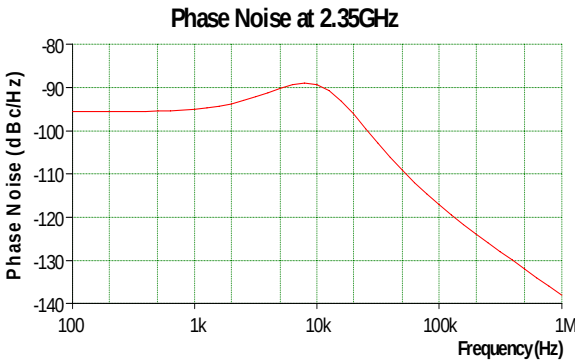

Figure 8. Closed loop phase noise simulation at 2.35 GHz

The PLL closed-loop in-band phase noise is –95 dBc/Hz and the rms phase error is only 0.35 degrees rms, equivalent to an EVM contribution of 0.6%.

POWER CONTROL AND RF POWER DETECTION

Because WiMAX systems can be used for non-line-of-sight applications, gain control of the transmitter is necessary to adjust the output TX level depending on the channel quality.

The VGA should provide linear high gain control range, with limited signal distortion and noise.

The ADL5330 is a high performance, voltage-controlled, variable-gain amplifier/attenuator for use in applications with frequencies up to 3 GHz. The balanced structure of the signal path minimizes distortion while it also reduces the risk of spurious feed-forward at low gains and high frequencies caused by parasitic coupling. While operation between a

balanced source and load is recommended, a single-sided input is internally converted to differential form.

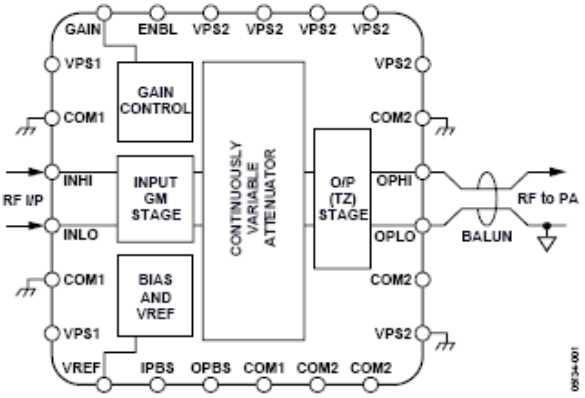

Figure 9. ADL5330 1 MHz to 3 GHz 60 dB Linear-in-dB VGA.

The input impedance is 50 Ω from INHI to INLO. The outputs are usually coupled into a 50 Ω grounded load via a 1:1 balun. A single-supply of 4.75 V to 5.25 V is required.

The 50 Ω input system converts the applied voltage to a pair of differential currents. The signal currents are then applied to a proprietary voltage-controlled attenuator providing precise definition of the overall gain under the control of the linear-in-dB interface. The GAIN pin accepts a voltage from 0 V at minimum gain to 1.4 V at full gain with a 20 mV/dB scaling factor.

The output of the high accuracy wideband attenuator is applied to a differential transimpedance output stage. The output stage sets the 50 Ω differential output impedances and drives Pin OPHI and Pin OPLO. The ADL5330 has a power-down function. It can be powered down by a Logic LO input on the ENBL pin. The current consumption in power-down mode is 250 μA.

In most cases, the VGA gain control is achieved through a closed loop system including a linear power detector. This helps relax the VGA linearity of the gain response. A single VGA in the transmit chain can achieve the required range of gain control. The part chosen for this purpose can maintain 50 dB of gain range, from –35 dB to +15 dB.

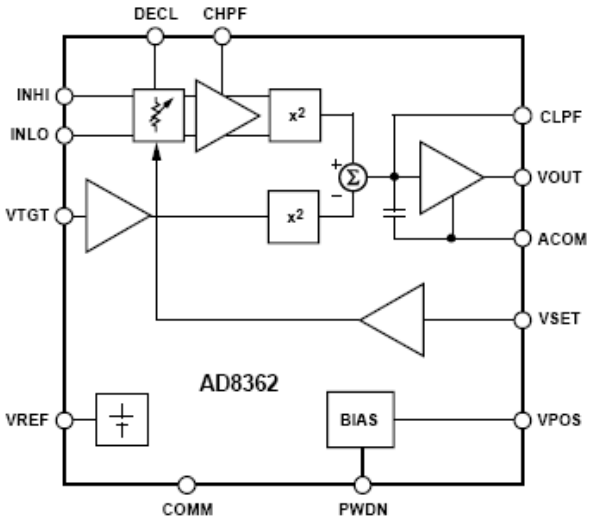

Figure 10. AD8362 50 Hz to 2.7 GHz 60 dB TruPwr™ Detector

The AD8362 is a true rms-responding power detector that has a 60 dB measurement range. It is intended for use in a variety of high frequency communication systems and in instrumentation requiring an accurate response to signal power. It is easy to use, requiring only a single supply of 5 V and a few capacitors. It can operate from arbitrarily low frequencies to over 2.7 GHz and can accept inputs that have rms values from 1 mV to at least 1 Vrms, with large crest factors, exceeding the requirements for accurate measurement of CDMA signals.

Used as a power measurement device, VOUT is strapped to VSET. The output is then proportional to the logarithm of the rms value of the input. In other words, the reading is presented directly in decibels and is conveniently scaled 1 V per decade, or 50 mV/dB; other slopes are easily arranged. In controller modes, the voltage applied to VSET determines the power level required at the input to null the deviation from the setpoint. The output buffer can provide high load currents.

For accurate and fast power control, an rms power detector is the most appropriate function to extract the rms power level of a non-constant envelope modulation signal with a variable peak-to-average ratio. It usually measures the output signal level of the power amplifier through a low loss directional coupler. The detector used here is a high accuracy, wideband rms-to-dc square law detector It achieves 40 dB (driven single-ended) to 60 dB (driven differentially) of detection range. Figure 11. shows the rms power measurement configuration technique which uses a directional coupler.

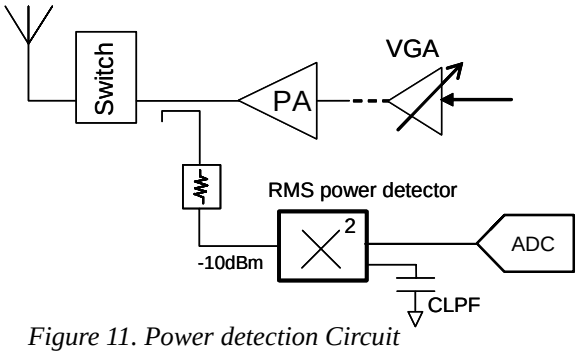

Figure 11. Power detection Circuit

Measured System Performance

The OFDM signal has been generated using ADS system/circuit simulation software from Agilent. Only 802.16d OFDM signal generation and demodulation capabilities were available at the time of the evaluation. EVM performance has been measured using the Agilent 89600 VSA software. The equalization was done using the channel estimation sequence only (the preamble) and the EVM results shown are higher than what they would actually be with equalization training on both preamble and data sequence.

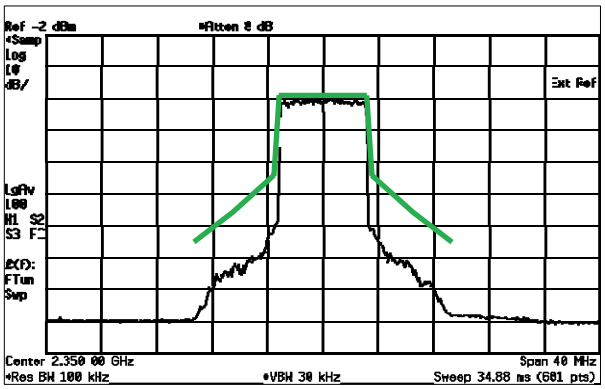

Figure 12. Spectral quality at 2.35GHz

The complete signal chain EVM performance as a function of the VGA gain or total output power level is given in Figure 13.

Table 1 summarizes the measured performance of the complete signal chain for a 10 MHz, 64QAM, 256-OFDM signal.

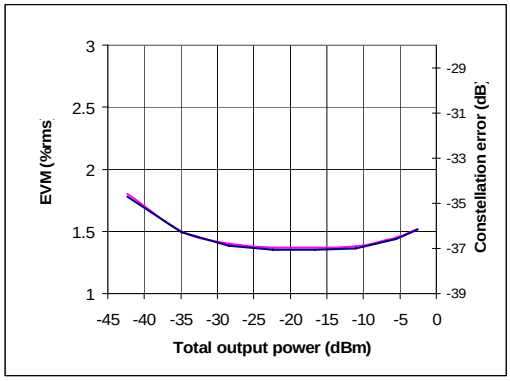

Figure 13. EVM function of gain control

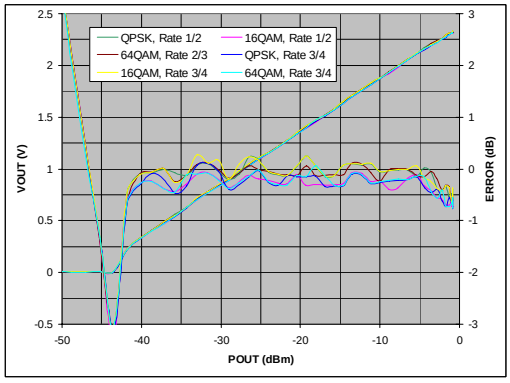

Figure 14. AD8362 RMS Detector Output Voltage and linearity error vs. System Output Power and Signal Type

Table 1

Max linear output power level	-1dBm
Power control range	50dB
Gain flatness	0.025dB/MHz
OP1dB	11dBm
OIP3	19.4dBm
Output noise at max gain	-142.5dBm/Hz
Output noise at min gain	-155dBm/Hz
Total EVM @-1dBm	1.7%
RMS power detection range (SE)	40dB
Detector response time	77us

The ADF4153 fractional-N PLL circuit used for this reference design has a total phase error due to phase noise of 0.35 degrees. This degrades the overall system EVM by 0.2%. Spectral quality is quite good for output power levels up to 0 dBm. As a reference, the WiBro mask is met with better than 15 dB margin at –3 dBm. The quality of these measured results demonstrates that this direct conversion architecture is viable to address the 2.5 GHz WiMAX systems requirements.